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French asynchronous design startup raises \$6.9 million

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(06/26/2009 3:47 AM EDT)

URL: <http://www.eetimes.eu/semi/218101472>

Tiempo AS, French startup specializing in the design of asynchronous ICs, announced it has raised 5 million euros (\$6.9 million) in a Series B financing round with venture capital firms Viveris Management and Oddo Private Equity and existing investors Emertec Gestion, Schneider Electric Ventures, INPG Entreprise SA and Alma Capital Finances.

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"The completion of this second financing round is an important milestone in Tiempo roadmap as it allows the company to complete its product development plan – IPs and synthesis tool – and to start the deployment of its sales and support channels worldwide," commented Serge Maginot, CEO of Tiempo.

[In June 2008](#), Tiempo raised 1.1 million euros (\$1.6 million) in an initial round of financing. The French startup then said the funds would be used to strengthen the development plan of the company's IP and EDA products but also to accelerate their commercialization worldwide.

Tiempo [recently](#) announced it would demonstrate the first synthesis tool for asynchronous logic that operates from standard design languages at the Design Automation Conference, due to be held July 27 to 30 in San Francisco.

The tool is called Asynchronous Circuit Compiler, or ACC, and it generates asynchronous and delay-insensitive circuits from a model written in a standard hardware description language. ACC takes as input a description written in SystemVerilog (IEEE Standard 1800-2005) as a Transaction-Level Model (TLM) and generates a gate-level netlist in standard Verilog format.

Tiempo was founded in July 2007 by Serge Maginot, former R&D director at Synopsys, Inc., and Marc Renaudin, former Professor at the National Polytechnical Institute of Grenoble (INPG) and former head of the CIS research group of the TIMA Laboratory (research labs from INPG, CNRS and Joseph Fourier University). The startup is located in Montbonnot Saint-Martin, near Grenoble (France).

To access Tiempo's website, click [here](#).

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