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Startup to demo synthesis of asynchronous logic at DAC

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LONDON — Tiempo AS (Grenoble, France) has said it will demonstrate the first synthesis tool for asynchronous logic that operates from standard design languages at the Design Automation Conference, due to be held July 27 to 30 in San Francisco.

The tool is called Asynchronous Circuit Compiler, or ACC, and it generates asynchronous and delay-insensitive circuits from a model written in a standard hardware description language. ACC takes as input a description written in SystemVerilog (IEEE Standard 1800-2005) as a Transaction-Level Model (TLM) and generates a gate-level netlist in standard Verilog format.

ACC also makes use of standard cell libraries, which can be augmented by Tiempo with a limited set of specific asynchronous cells for better power/speed/area performances. These unique properties allow ACC to be inserted in a standard design flow, the company claimed. The use of SystemVerilog allows designers to verify asynchronous and mixed asynchronous-synchronous circuits using standard simulation tools, the company also asserted.

Predefined asynchronous channels and asynchronous/synchronous interface components, modeled in standard SystemVerilog, as well as a recommended coding style for synthesis, are provided by Tiempo allowing high-level modeling of asynchronous circuits. The generated Verilog netlist can be placed-and-routed using standard back-end tool and verified with static timing analysis and electrical simulation tools.

ACC solves traditional asynchronous methodologies limitations, finally bringing to the designer community the benefits of asynchronous circuits (ultra-low power, ultra-low voltage, etc.) while using a standard design flow. ACC is currently being used by Tiempo engineers for the design of Tiempo asynchronous ultra-low power core IPs, such as microcontroller and crypto-processor cores.

As an example, TAM16, Tiempo 16-bit microcontroller core released in November 2008, consumes as little as 37-microamps per MIPS when operating at 0.7-V (47-microamps at 1.2 V), including leakage current in a CMOS 130-nm general-purpose process.

ACC is available to Tiempo IP customers as an optional license attached to any Tiempo core IP license, allowing the customers to independently modify the purchased IPs as well as to synthesize customer-specific asynchronous blocks complementing these IP blocks.

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